PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/20/12147

Analog, MEMS & Sensors (AMS)

Introduction of a new Assembly and Test location (TSHT China) for products assembled in SOT23 5L package

WHAT:

Progressing on activities related to process modernization and quality improvement, ST is pleased to announce the introduction of TSHT/China as an added subcontractor for Assy and Test & Finishing activities for some products assembled in our SOT23 5L package. **We already released in July 2017 the PCN10331 and 10454 announcing this new plant.** This new PCN is just to enlarge the list of impacted products.
The list of test vehicles used for the validation is listed here below.

Commercial Product	Current Finished Good	Current Assy & TnF Plant	Added Finished Good	Added Assy & TnF Plant
LD2981CM33TR	LD2981CM33TR$2V	Carsem	LD2981CM33TR$1R	TSHT
LDK120M-R	LDK120M-R$3V	Carsem	LDK120M-R$1R	TSHT

Dedicated engineering trials and test vehicles have been defined to validate the change.

WHY:
The purpose of the introduction of TSHT for both Assy and Test & Finishing activities for the here above listed commercial products is to further improve the rationalization of our manufacturing assets and provide a better support to our customers by enhancing the manufacturing process for higher volume production.

HOW:
•The qualification is based on Test vehicle representatives by using internal ST rule for changes.

WHEN:
The transfer set will be implemented in Q2/2020 in TSHT.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities.
Shipments may start earlier with the customer's written agreement.

Reliability Qualification plan

New Subcontractor

SOT23 in SC-Tianshui Huatian-China (TSHT)

TVs: LDK120 (UI69) & LD2981(KR33)

General Information	
Product Lines	UI69
Product Description	200 mA low quiescent current very low noise LDO
P/N	*LDK120M-R$4V*
Product Group	*AMG (Analog & MEMS Group)*
Product division	*General Purpose Analog & RF Division POWER MANAGEMENT*
Package	***SOT23 5L - 1.0mil Pd-Cu***
Silicon Process technology	*BCD6S*

Locations	
Wafer fab	*CTM8*
Assembly plant	***SC-Tianshui Huatian-China (TSHT)***
Reliability Lab	*Catania Reliability LAB*

General Information	
Product Lines	KR33
Product Description	Very Low Drop VREG @ 100mA 3.3 V
P/N	*LD2981ABM33TR$3V*
Product Group	*AMG (Analog & MEMS Group)*
Product division	*General Purpose Analog & RF Division POWER MANAGEMENT*
Package	***SOT23 5L - 1.0mil Pd-Cu***
Silicon Process technology	*BI20II*

Locations	
Wafer fab	*Singapore 6*
Assembly plant	***SC-Tianshui Huatian-China (TSHT)***
Reliability Lab	*Catania Reliability LAB*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Jun-2017	7	Giuseppe Failla	Giovanni Presti	Final Report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the SOT23 in the subcontractor SC-Tianshui Huatian-China (TSHT)
In order to cover the FE/BE compatibility two TVs in different technologies have been chosen:

- TV1: LDK120M-R$4V (UI69) diffused in BCD6S
- TV2: LD2981ABM33TR$3V (KR33) diffused in BI20II.

BE Process
To be qualified
3 different Lots + 2 different BE CLs for each Test Vehicle are requested

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime

4 DEVICE CHARACTERISTICS

4.1 Device description

- The LDK120 low drop voltage regulator provides 200 mA of maximum current from an input supply voltage in the range of 1.9 V to 5.5 V, with a typical dropout voltage of 100 mV. It is stabilized with a ceramic capacitor on the output.
  The very low drop voltage, low quiescent current and low noise features make it suitable for low power battery powered applications. An enable logic control function puts the LDK120 in shutdown mode allowing a total current consumption lower than 1 µA. The device also includes a short-circuit constant current limiting and thermal protection.

- The LD2981 is a 100 mA fixed-output voltage regulator. The low-drop voltage and the ultra low quiescent current make them suitable for low noise, low power applications and in battery powered systems.
  The quiescent current in sleep mode is less than 1 µA when INHIBIT pin is pulled low. Shutdown logic control function is available on pin n° 3 (TTL compatible). This means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption.
  The LD2981 is designed to work with low ESR ceramic capacitor. Typical applications are in cellular phone, palmtop/laptop computer, personal digital assistant (PDA), personal stereo, camcorder and camera.

4.2 Construction note

	LDK120M-R$4V (UI69)	LD2981ABM33TR$3V (KR33)
Wafer/Die fab. information		
Wafer fab manufacturing location	CT8	AMK6
Technology	BCD6S	BI20II
Die finishing back side	RAW SILICON	LAPPED SILICON
Die size	782 x 736 um	1470 x 990 um
Bond pad metallization layers	Ti/AlCu/TiNARC	AlSi
Passivation type	TEOS/SiN/Polyimide	P-Vapox/Nitride/Polyimide(PIQ)
Assembly information		
Assembly site	SC-Tianshui Huatian-China (TSHT)	
Package description	SOT 23 5L	
Molding compound	Epoxy	
Frame	SOT235 A194 (52X72) -16P	
Die attach process	GLUE	
Wires bonding materials/diameters	1.0mil Pd Cu	
Lead finishing process	Pure Tin Plating Sn 100%	

5 TESTS PLAN SUMMARY

5.1 Test plan and results summary

TV1: LDK120M-R$4V (UI69)

Test	PC	Std ref.	Conditions		Steps	SS				
						Lot 1	Lot 2	Lot 3	Lot 1-CL	Lot 1-CL
Die Oriented Tests (*)									LL parameter	HH parameter
HTOL		JESD22 A-108	Tj = 125°C, V= Vbias +7V		168 H	0/77				
					500 H	0/77				
					1000 H	0/77				
HTSL		JESD22 A-103	Ta = 150°C		168 H	0/25	0/25	0/25	0/25	0/25
					500 H	0/25	0/25	0/25	0/25	0/25
					1000 H	0/25	0/25	0/25	0/25	0/25
Package Oriented Tests (*)										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	pass	pass	pass	pass	pass
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 h	0/25	0/25	0/25		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy	0/25	0/25	0/25	0/25	0/25
					200cy	0/25	0/25	0/25	0/25	0/25
					500 cy	0/25	0/25	0/25	0/25	0/25
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Bias +5,5V		168 H	0/25	0/25	0/25		
					500 H	0/25	0/25	0/25		
					1000 H	0/25	0/25	0/25		
Other Tests										
ESD		JESD22-C101	CDM		500V 750V corner pins	Pass				
CA			Construction Analysis			Pass				

Note (*) All samples have been assembled on dedicated PCB in agreement with JEDEC020 spec.

TV2: LD2981ABM33TR$3V (KR33)

Test	PC	Std ref.	Conditions		Steps	SS				
						Lot 4	Lot 5	Lot 6	Lot 4-CL	Lot 4-CL
Die Oriented Tests									LL parameter	HH parameter
HTOL		JESD22 A-108	Tj = 125°C, V= Vbias +20V		168 H	0/77				
					500 H	0/77				
					1000 H	0/77				
HTSL		JESD22 A-103	Ta = 150°C		168 H	0/25	0/25	0/25	0/25	0/25
					500 H	0/25	0/25	0/25	0/25	0/25
					1000 H	0/25	0/25	0/25	0/25	0/25
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	pass	pass	pass	pass	pass
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 h	0/25	0/25	0/25		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy	0/25	0/25	0/25	0/25	0/25
					200cy	0/25	0/25	0/25	0/25	0/25
					500 cy	0/25	0/25	0/25	0/25	0/25
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Bias +16V		168 H	0/25	0/25	0/25		
					500 H	0/25	0/25	0/25		
					1000 H	0/25	0/25	0/25		
Other Tests										
ESD		JESD22-C101	CDM		500V 750V corner pins	pass				

Note:

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.